Datasheet and User Manual
FT015
Power On Delay RevA

2/26/2014

Features

The FT015 is designed primarily for use with MultiWriter. It provides a settable delay for the input power line for cases where power must be applied after other signals on the IC. This is necessary for devices that must enter programming mode off of a POR.

Operational Characteristics

General Usage

The FT015 has one settable delay, but four independent channels. Although the delay setting is shared, each channel has an independent timer.

On board switches will set the delay from the input to the output pin.

Trigger inputs are meant to be tied to the MultiWriter RLY lines.

Falling edge on trigger inputs will start the timer. When timer value equals the value of the switch settings the input voltage will switch through to the output voltage.

Rising edge on trigger inputs will reset the timer.

Input channels can be tied together, but output channels should not be. Based on the way the MultiWriter switches the relay lines, it is necessary for each UUT to have a separate power source. This means that power must not be shared between buffers, and any two UUTs on an x2 buffer should be powered separately from the PWR1 and PWR2 liens.

I/O Pin Descriptions

P1 INPUT
P1 connector has:
a. General board power
b. 4 Power inputs for delay channels
c. Trigger inputs for delay channels

P1 PINOUT

PIN	NAME	FUNCTION
1	RLY1	Trigger in channel 1
2	VIN1	Power in channel 1
3	RLY2	Trigger in channel 2
4	VIN2	Power in channel 2
5	RLY3	Trigger in channel 3
6	VIN3	Power in channel 3
7	RLY4	Trigger in channel 4
8	VIN4	Power in channel 4

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P2, P3 OUTPUT

Delayed output voltages. This header is intended to interface to J1 header on the 105/107 buffers

P2 PINOUT

PIN	NAME	FUNCTION
1, 2	PWR1	Delayed power out channel 1
3, 4	GND	Ground for Buffer#1
5, 6	PWR2	Delayed power out channel 2

P3 PINOUT

PIN	NAME	FUNCTION
1, 2	PWR1	Delayed power out channel 3
3, 4	GND	Ground for Buffer#2
5, 6	PWR2	Delayed power out channel 4

P8 PROGRAMMING HEADER

The programming header is designed to directly plug into the Digilent HS1 Rev. A JTAG programming cable. Board power must also be supplied. If another programmer is used it must provide 1.8V logic levels.

P8 PINOUT

PIN	NAME	FUNCTION
1	+1V8	Logic level sense
2	GND	Ground
3	TCK	JTAG TCK
4	TDO	JTAG TDO
5	TDI	JTAG TDI
6	TMS	JTAG TMS

P7 PINOUT

This header provides power to the power-on delay board

P7 PINOUT

PIN	NAME	FUNCTION
1	+5V	Board power
2-5	GND	Ground

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P4 PINOUT

This header is to be loaded with jumpers in the 1-8 position in order to provide a bit pattern to the module, which is then interpreted into a delay time as shown in the following table.

P4 JUMPER SETTINGS

SW PIN	TIME DELAY
1	4ms
2	8ms
3	16ms
4	31ms
5	63ms
6	125ms
7	250ms
8	500ms

Programming Requirements

CPLD XC2C64A must be programmed through the JTAG header.

Communication Busses

None

Truth Table

DNA

AC DC Requirements

	Min	Nom	Max	Units
Vpwr	2.2	5	16	V
Ipwr	-	-	2	mA
VIN	1.8	-	30	V
VIL (RLY)	-0.5	0	0.43	V
VIH (RLY)	0.97	-	-	V
VIL (JTAG)	-0.3	0	0.63	V
VIH (JTAG)	1.17	1.8	2.1	V
Timer error	-	-	4	ms

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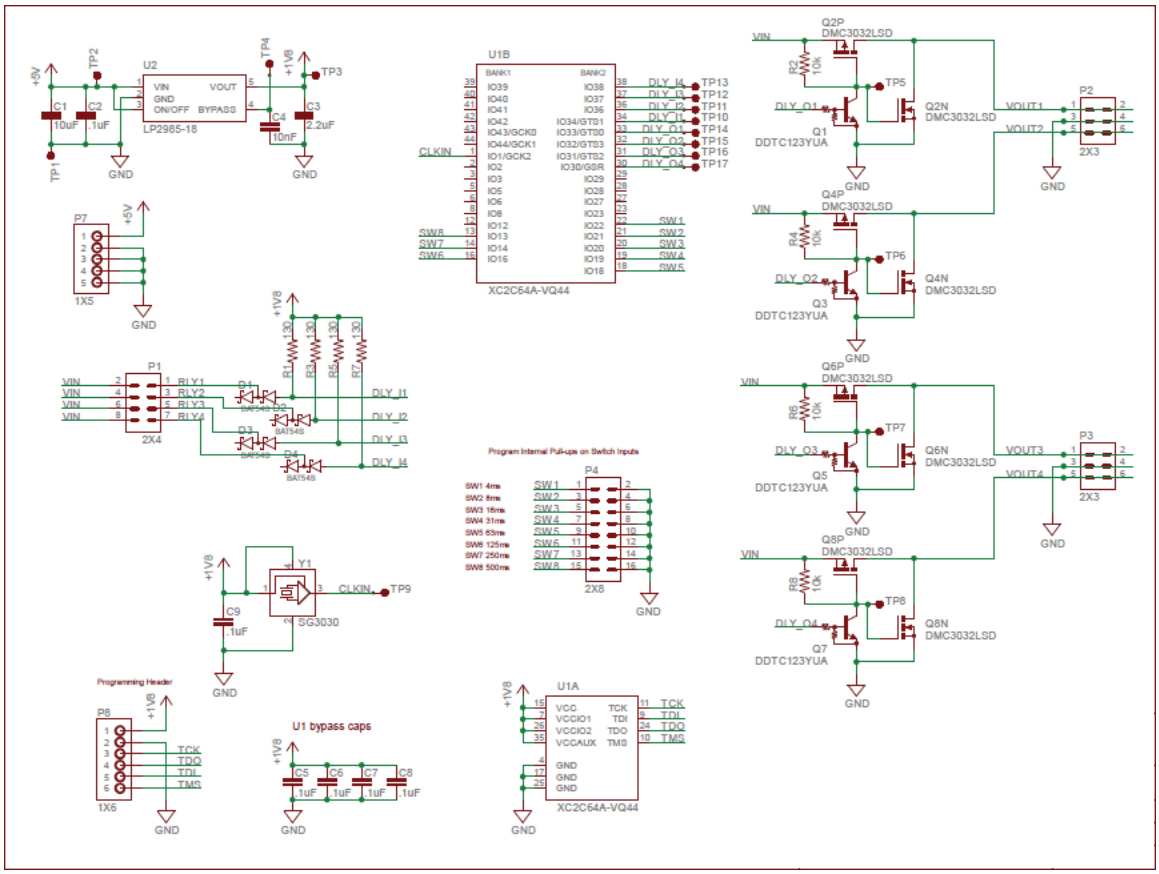
Schematic and Board Layout

Schematic



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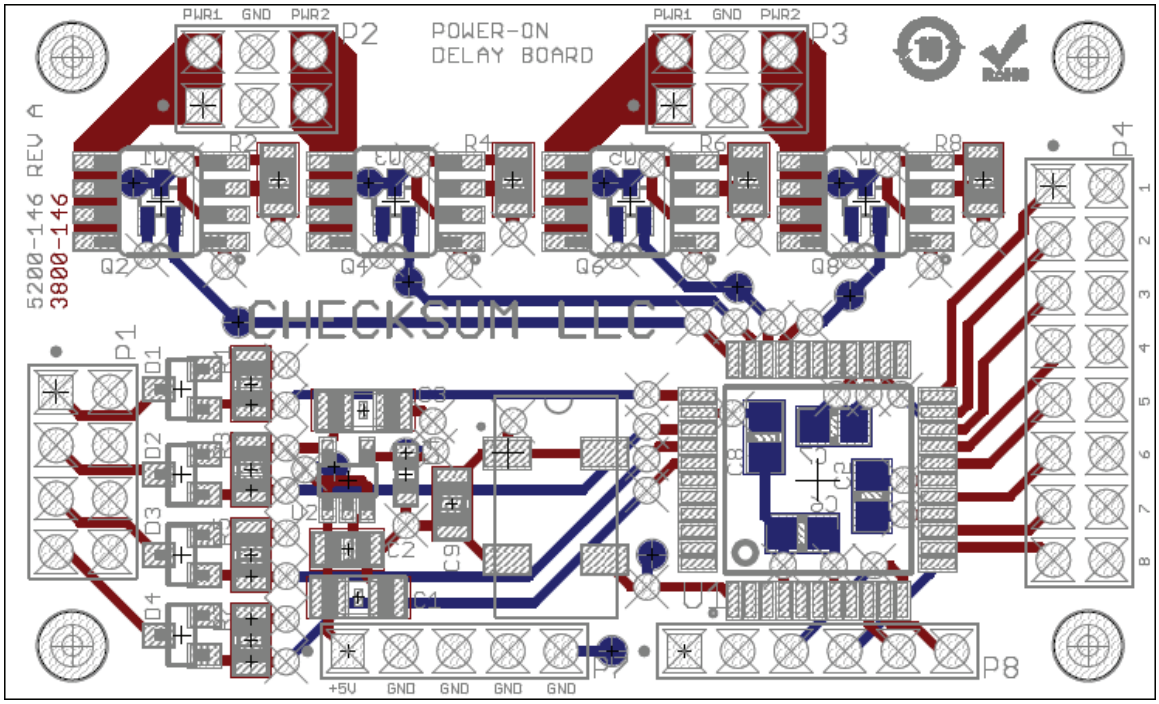
PCB Layout



Board Dimensions & Mounting

Board outline 2.15” x 1.3”
Mounting holes (0.125”,0.100”) (2.025”,0.100”) (0.125”,1.200”) (2.025”,1.200”)
Drill size .126”

Parts Listing

Qty	Part#	Value	Reference Designator	Device
1	3800-146 Rev-	PCB, Delay board		

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Surface Mount

6	1000-092	.1uF	C2, C5, C6, C7, C8, C9	C_0805
1	1000-100	2.2uF	C3	C_1206
4	0805-006	10k	R2, R4, R6, R8	R_0805
1	0603-002	10nF	C4	C_0603
1	1000-098	10uF	C1	C_1206
1		32.768kHz	Y1	SG3030
4	0805-033	130	R1, R3, R5, R7	R_0805
4	1500-230	BAT54S	D1, D2, D3, D4	BAT54S
4		DDTC123YUA	Q1, Q3, Q5, Q7	DDTC123YUA
4		DMC3032LSD	Q2, Q4, Q6, Q8	DMC3032LSD
1		LP2985-18	U2	LP2985-18
1		XC2C64A-VQ44	U1	XC2C64A-VQ44

Through Hole

1	1020-011	2X4-100	P1	2X4-100
1	1020-011	1X3-100	P2	1X3-100
1	1020-011	1X3-100	P3	1X3-100
1	1020-011	2X8-100	P4	2X8-100
1	1020-011	1X5-100	P7	1X5-100
1	1020-011	1X6-100	P8	1X6-100

Glossary

References

XC2C64A datasheet
LP2985-18 datasheet
PowerOnDelay.vhd source code