MultiWriter™ On-Board Programming

Higher Throughput. Lower Cost. Solving the ISP Productivity Bottleneck.

The ISP Challenge in Circuit Board Assembly and Test

As product life cycles shorten and cost pressures mount, circuit designers are using In-System Programmable (ISP) devices such as embedded microcontrollers, serial Flash and FPGAs on just about every type of board. ISP chips let designers add enhanced features to new products with minimal hardware redesign.

ISP design proliferation means that the chips must be programmed before or after they are soldered to the board. Logistics and inventory considerations almost always point to programming the ISP chip after it's been attached to the board.

Unfortunately, today's existing ISP programming solutions are almost always too slow, too expensive—or both—for high-volume manufacturing. This is especially true when manufacturing multi-board panel assemblies, which are increasingly popular in today's PCB assembly environment of high volumes and shrinking board sizes.

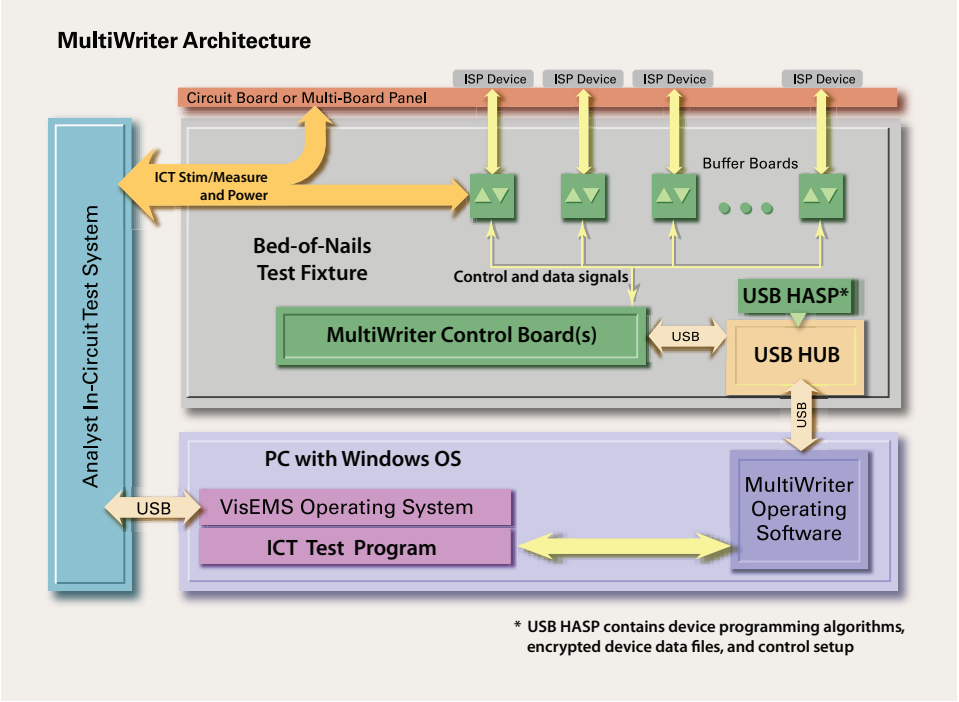
Most dedicated chip programmers are not an option because they do not meet the requirements of high-speed assembly lines. Typically, they can program only one device at a time and are simply too slow to keep up with the line beat rate.

Many production engineers have turned to in-circuit testers (ICT) as an ideal platform for programming on-board ISP devices. The bed-of-nails (BoN) fixture provides ready access to the device and when appropriately equipped, ICT channel cards are architecturally suited to ISP programming functions. However, ICT systems are expensive—even more so when equipped with ISP programming capability. Add in the high-priced BoN fixturing required by these testers, and the increased throughput offered by traditional ICTs often comes at too high a cost.

The manufacturing engineer's dilemma is stark: one way or the other, today's in-line ISP solutions are a productivity bottleneck.

MultiWriter Reduces Cost While Multiplying Throughput

The MultiWriter™ ISP System is the logical in-line, ICT-based ISP programming solution to the productivity dilemma. Integrated with CheckSum's Analyst™ low-cost ICT, MultiWriter solves the productivity bottleneck by programming multiple ISP chips simultaneously at near data-book speeds—all at a substantially lower price point than other ICT-based approaches. This advanced design delivers a significant throughput advantage over both standalone ISP programmers



Installing the ISP Control Module and one or more buffer modules inside the test fixture adds complete ISP programming capability to the Analyst in-circuit tester. No expensive tester-based hardware is required.

MultiWriter's Throughput Speed: How Fast Is It?

The primary design goal of the MultiWriter ISP System is to enhance throughput where it matters most–in the production line. Here's an example of MultiWriter's programming time for a single device or several chips simultaneously.*

Device Type: 25LC640 Serial EEPROM
Memory Size: 8K Byte
Serial Bus type: SPI at 2 MHz

Benchmark Results:

Programming Time for a Single Device:	
Software Overhead:	1.16 Seconds
Programming Time:	0.65 Seconds
TOTAL	1.81 Seconds

Four Devices Programmed in Parallel:	
Software Overhead:	1.16 Seconds
Programming Time (4-Up):	0.69 Seconds
TOTAL	1.85 Seconds

Verification Time for a Single Device:	
Software Overhead:	1.16 Seconds
Verification Time:	0.10 Seconds
TOTAL	1.26 Seconds

Verification Time for Four Devices in Parallel:	
Software Overhead:	1.16 Seconds
Verification Time:	0.10 Seconds
TOTAL	1.26 Seconds

* Many factors can affect actual throughput; actual results will vary.

Example Devices That Can Be Programmed by MultiWriter

- I2C Serial EEPROMs (e.g. 24LC00) Microchip, Atmel
- SPI Serial EEPROMs (e.g. M95256) STMicroelectronics
- Microwire – (e.g. 93LC32) Microchip
- JTAG programming, CPLDs from Atmel, Xilinx, Altera and Lattice (e.g. Xilinx XC9572, Altera EPM3064)
- Flash Microcontrollers:
  Microchip (e.g. PIC16F877, PIC18F248)
  Atmel AVR (e.g. AT90S8535)
  Atmel ATmega (e.g. ATmega32)
  Atmel ATtiny (e.g. ATtiny15)
  STMicro ST7 STM8, STM32
  Hitachi H8
  Renesas H8S, M16, R8C family
  Freescale HC908, HC912, and Star12
  TI TMS470, MSP430
  NEC 78K, V850

and traditional in-circuit testers–in both overall throughput and serial programming speed.

MultiWriter uses unique, patented† technology to program up to 384 serial bus ISP devices simultaneously in a single pass. Whether you have a single chip on a single board or multiple chips per board on a multiple-board assembly or any combination in between, the total programming time will be identical. In addition, MultiWriter programs serial Flash, EEPROMS, embedded microcontrollers, and FPGAs at near-data book speeds.

Following CheckSum's design philosophy of developing straightforward products that simplify customer processes and reduce manufacturing cost, MultiWriter is the first ICT-based ISP system designed specifically for popular serial-bus programming protocols. Working integrally with CheckSum's Analyst™ ICT product line, MultiWriter reduces cost because it eliminates the hardware and software overhead and complexity required for rarely needed parallel-bus programming. In addition, serial-bus programming is the key to achieving programming speeds that are essentially the fastest cited in the part's published specification sheet.

MultiWriter's unique hardware and software architecture not only reduces cost while multiplying throughput it also simplifies application. CheckSum provides ISP programming capability by putting it into the fixture, rather than in the test system. MultiWriter hardware resides right in the Analyst BoN test fixture—eliminating the need for complex and expensive system channel cards and shortening signal path length for improved signal integrity. Its application library includes bus algorithms for a host of popular ISP device families.

Like CheckSum's Analyst ICT systems, every aspect of MultiWriter is aimed a single goal: increasing manufacturing productivity and reducing cost.

The MultiWriter design approach is far more economical than that of traditional in-circuit test systems, which rely on expensive channel cards to deliver ISP programming functionality. In addition, with MultiWriter, ISP programming capability can be added on a project or per-board basis, providing more flexibility. The flexible architecture of the Analyst ICT system enables CheckSum to respond to customers' needs and adapt to changing technologies.

MultiWriter ISP Programming Structure & Process

Board Design Considerations

As is the case in most designs, the circuit design must allow in-system programming such that the device can be programmed without the requirement to overdrive other signals. The ISP device programming pins must be accessible via a bed-of-nails fixture—just like any other in-circuit test point.

The board or multi-board panel assembly layout should provide electrical access to the programming pins that are as physically close as possible to the device being programmed in order to minimize cross-talk and noise.

Device Programming Considerations

MultiWriter allows unique data such as a date code or serial number for the parts to be programmed with minimal impact on programming time. The part serial number or other data such as an assembly serial number entered via bar code can be stored in a file or provided at run-time. Calibration or other measurement data can be programmed into

† MultiWriter Technology is protected under U.S. Patent No. 7,802,021.

each part separately. Since unique data is typically a very small portion of the overall part memory, the programming time for chip-unique data will be minimal.

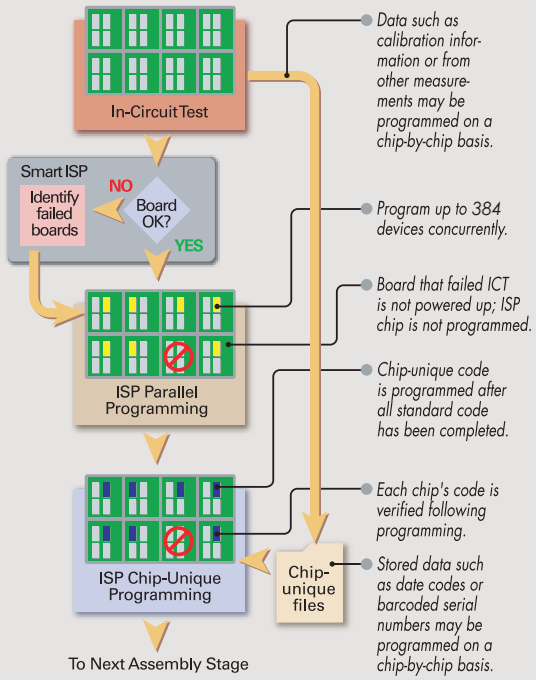
A standard data file format (INTEL hex, Motorola S-Record, SVF, STAPL) is used for storage of unique data that is accessed during the ISP programming process.

The MultiWriter Controller board has two operating modes: Program and Verify. In Program mode, the controller places the ISP chip in the "program" state and code appropriate to the device is retrieved from the computer memory and applied via the fixture-based buffer boards. Once chip programming is complete, the MutliWriter controller places the chip in the "read" state and the code just programmed is verified. The Program and Verify operations can occur on a Test Step basis.

The board assembly (or individual panel in a multi-up assembly) will be powered-up to program the part, so a sufficient board power source must be available at the test system.

Smart ISP. MultiWriter's Smart ISP™ technology ensures that the ISP programming phase follows a defect-free in-circuit test of the board. The test system programs only boards that have passed the in-circuit tests. Only assemblies that have passed the opens/shorts and other component tests are powered-on. For example, if a panel has seven tested-good assemblies out of eight total (as illustrated in the figure left), then only those seven will be powered-on for ISP device programming.

The MultiWriter ICT Test and ISP Programming Process



ISP programming follows a power-off in-circuit test. Smart ISP™ ensures that board power is applied only to those boards in a multi-board panel assembly that have passed the in-circuit test, ensuring that components are not inadvertently damaged. Standard code for all ISP parts is programmed simultaneously followed by chip-unique program code on a per-device basis.

Low-Cost ICT: Save Money by Reducing Complexity

In the late 1980s, when cell phones were the size of shoeboxes and PDAs existed in imagination only, test engineers relied on high-capability in-circuit testers (ICT) like the HP (now Agilent) 3070 and the GenRad 2280-Series. Test engineers needed ICT loaded with every possible test technique and capability in order to find a wide variety of analog and digital faults in processes whose yields were frequently less than 75%.

Circuit boards and the manufacturing processes that build them have come a long way since then. Today, SMT is the norm, and complex mixed-technology chips like SOC occupy smaller, denser boards. Process yields are routinely 95%. The fault spectrum has shifted from shorts to opens, with fewer analog faults and almost no digital defects.

The Problem with Using "Big Iron" ICT in Today's Processes

Despite these major changes in device, board, and process technologies, many test engineers still insist on using traditional "big iron" ICT for every project and every board. This is true even though today's boards rarely require capabilities such as high-accuracy analog and digital backdrive. Why? The low failure rates of today's "jellybean" ICs has made digital backdrive tests effectively superfluous, and vector-based tests for complex ICs such as SOCs are exorbitantly expensive and time- consuming (and frequently impossible) to write. As a result, the actual test programs that run on a traditional ICT today almost always exclude complex analog or digital tests. Nevertheless, many test engineers argue that the extra capabilities are an insurance policy—there when needed "just in case."

It may seem that having for this extra "tester insurance" makes sense, but the insurance comes with a price. Even when their excess capability is left unused, "big iron" testers cost more to own and operate. The inherent complexity of fixtures, programs, and maintenance for these systems still drives up costs significantly—even when the tester itself is "free." Estimates place the annual excess cost of using traditional ICT instead of lower-cost testers at more than $250 million in North America alone. This is money that is spent needlessly when excess tester capability is not matched to the reality of higher yields and today's new fault spectrum.

The CheckSum Difference

CheckSum's Analyst low-cost ICT systems match the requirements and the fault spectrum of today's higher-yield processes. Unnecessary and unused capabilities—and their associated complexity and costs—are omitted. Not only is the price of Analyst systems a fraction of traditional ICT, more importantly, ongoing operating costs (fixtures, programs, and support) are typically 50% less. Our focus on minimizing fixture cost and simplifying programming saves money each time a new test job comes on line. Electronics manufacturers who switch over to CheckSum systems find the cost savings to be immediate and dramatic.

MultiWriter carries CheckSum's cost-saving philosophy into the realm of on-board ISP programming: omitting superfluous capability while maximizing productivity across each board and each project.

Key Features & Benefits

ICT-based in-line ISP programming at lower cost:

- MultiWriter ISP programming and verification is part of a fully-integrated system that also includes the bed-of-nails fixture and in-circuit test program in a complete, ready-to-run package.
- Designed for high-volume production environments, the MultiWriter system employs the same process used on today's traditional in-circuit testers to program ISP devices after they've been soldered to the board—but at a fraction of the system, fixturing, and programming costs.

The MultiWriter ISP System is appropriate for circuit boards and multi-board panel assemblies requiring on-board code programming and verification of serial bus ISP devices. MultiWriter is available only as an integrated element of a CheckSum-developed application package that includes a bed-of-nails fixture and associated test program operating on an Analyst in-circuit test system.

MultiWriter is the first ISP programming system integrated right into the bed-of-nails fixture.

- Fixture-based architecture delivers maximum flexibility at the lowest possible cost.
- Eliminates the requirement for expensive tester channels and long signal paths.

Simultaneous device programming

- Up to 384 ISP devices* whether on a single board or distributed across multiple boards in a panel assembly, and all combinations in between, are programmed simultaneously.
- Flexible code verification can be performed after all programming is complete or on a step-by-step basis.
- Boards need not be de-paneled prior to programming ISP devices.

Comprehensive device and bus algorithm library

- Currently supported bus algorithms include I2C, SPI, Microwire, JTAG, and PIC, with more under development.
- MultiWriter's architecture supports user-defined algorithms, as well.

Smart ISP™ ensures failed boards are not programmed—even when part of a multi-up assembly.

- With CheckSum's Smart ISP technology, there's no possibility of damaging expensive components. Power is applied only to boards or individual boards within a multi-board panel assembly that has passed the ICT opens/shorts and other component tests.

Unique data may be programmed on a per-device basis—even on panelized boards.

- MultiWriter handles data unique to each device such as serial number or board calibration information
- Data collected on-the-fly at earlier test stages may be manipulated (i.e., calculations performed) and then programmed directly into the device during the same test sequence.

Fixture-mounted buffer boards ensure the highest signal quality.

- A buffer board associated with each device to be programmed delivers clean signals and state conditioning at the highest possible programming speed.
- Buffer boards are mounted right in the fixture, eliminating cabling problems and ground return issues for noise-minimized reliability.

User Data Protection Encryption Option

- An optional data protection encryption software package is available that makes the contents of the device file not readable without the encryption key. This protection system also prevents production personnel from modifying the device data.

* Up to 16 MultiWriter control modules with up to 24 buffer modules each for 384 maximum devices. One MultiWriter control module required for each unique device bus algorithm.

Specifications

System Computer Interface

- USB 1.1 or USB 2.0. Recommend USB 2.0 for max. speed and throughput.
- Requires CheckSum Analyst *ems* test system software running in a Windows OS environment.

Supported Part Families with Serial Programming Bus Algorithms

- 24LCXX (I2C) and 25LCXX (SPI)
- 93CXX (Microwire)
- Atmel ATmega and ATtiny families
- Cypress CY8C21XXX/C24XXX (ISSP)
- Microchip PIC 12F, 16F, 18F, dsPIC30F
- Freescale HC908, HC912, Star12 (UART/BDM) & MPC5X (JTAG)
- STMicro M24/25, M34/35, M93/95, ST7, STM8, STM32 (SWIM/JTAG/USART)
- Hitachi H8 and Renesas H8S, M16, R8C family (USART/UART)
- TI TMS470, MSP430
- NEC 78K0, V850 and Xilinx CoolRunner II/XPLA3 CPLD family
- Zilog Z8 family

ISP Controller Board

- Controller board is connected to computer via USB 2.0, which also powers the board. Requires "high power" USB 2.0 rated hub. Board draws approximately 150 mA unloaded.
- Board dimensions: Approximately 3" x 5.5" / 8 cm x 14 cm, mounted in bed-of-nails test fixture.

ISP Buffer Board

- Driver Voltage: 3.3V or resistor programmable for lower voltages
- Nominal output impedance: 200 Ohms (buffer to device)
- Nominal sensor input impedance: >100K Ohms (device to buffer)
- Twisted pair wiring between buffer driver/sensor and device.
- Buffer board nominal power supply requirement: +12V, +5V (usually provided by PWR-2 Module).
- Driver/sensor buffer boards are mounted in a bed-of-nails test fixture.
- Buffer board: Single 2.125" x 2.125" (5.4 cm x 5.4 cm), 4-up 2.125" x 8.75" (5.4 cm x 22.23 cm)

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